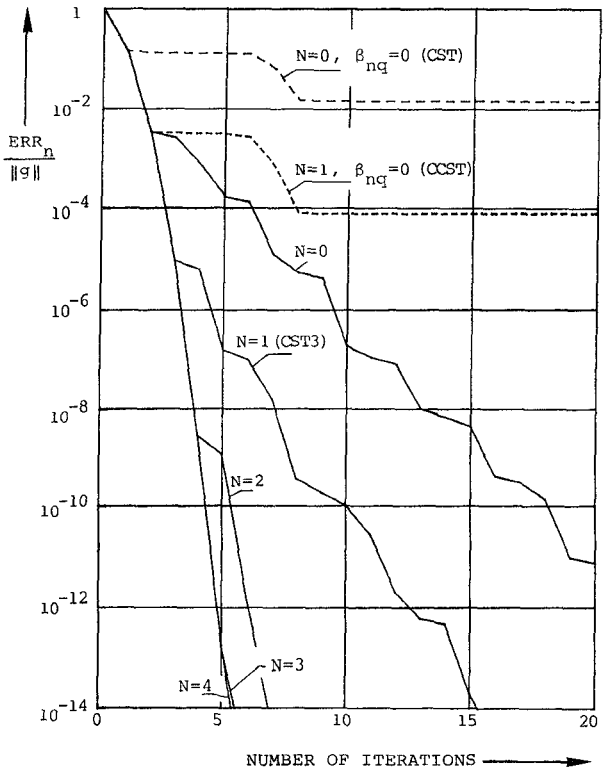

Fig. 5. The normalized error ERR_n as a function of the number of iterations for the electric field problem of an interdigital transducer.

where N is the number of correction functions taken into account. The scheme for $N=1$ is the CST3 scheme [4], [6]. The broken lines represent the results of the incomplete orthogonalization scheme if we enforce the value of β_{nq} of the second term of (13) to zero. In this latter case, the two schemes for $N=0$ and $N=1$ coincide with the so-called CST and CCST schemes [3], [7], respectively.

To conclude we observe that a full orthogonalization of all basis functions is in many cases no longer necessary when the incomplete orthogonalization scheme is followed. It appears that the CST3 scheme is a very efficient computational scheme, in view of achieving the right balance between computer memory and computer time. Another approach is one in which the available computer determines the number of correction functions that will be taken into account in our incomplete orthogonalization scheme. The available computer memory for the user is the upper limit of this number of correction functions.

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High-Speed GaAs Dynamic Frequency Divider Using a Double-Loop Structure and Differential Amplifiers

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Abstract—**New GaAs 2.0–8.0 GHz and 6.0–10.5 GHz dynamic frequency dividers have been developed. These dynamic dividers have a double-loop structure using a differential amplifier for high-speed and stable operation despite supply voltage fluctuations. This structure operates from one voltage supply. An advanced WSi self-aligned gate process technology (1.0 μm long gate) was used to improve the high-frequency characteristics of the FET.**

I. Introduction

Satellite and multiplex communication systems need oscillators of small size and high stability. High-performance phase-locked oscillators can satisfy these demands, but require the development of high-speed frequency dividers. Dynamic frequency dividers can operate at a higher frequency than static ones, because their propagation delay time is shorter [1]–[3]. However, because of the direct-coupled feedback circuit and the use of a common-source FET for the inverter, they are sensitive to supply voltage fluctuation, and cannot operate at variations of ±10 percent. Such conventional dividers require many power supplies.

This paper describes a newly developed dynamic frequency divider that overcomes these problems without sacrificing speed. This divider was constructed by connecting differential amplifiers in a double loop. This structure provides stable operation insensitive to supply voltage fluctuation, and moreover it achieves single supply operation. WSi self-aligned structure gate process technology was used to produce the IC for ease of mass production [4]. We have produced 2.0–8.8 GHz and 6.0–10.5 GHz dynamic dividers.

II. Circuit Design

The fundamental circuit configuration of the dynamic frequency divider is shown in Fig. 1. The common-source inverter was replaced by differential amplifier A. Also, the source follower buffer was replaced by differential amplifier B for more gain. A schematic of the differential amplifiers is shown in Fig. 2(a). The diode over the load resistor regulates proper drain–source voltage for high-level operation of the level-shift FET's (C, D). The self-biasing circuit was used to determine the input dc level for proper operation as shown in Fig. 2(b). A two-stage output buffer was adopted to retard reduction of the operating frequency. The first stage used a small gate width buffer for

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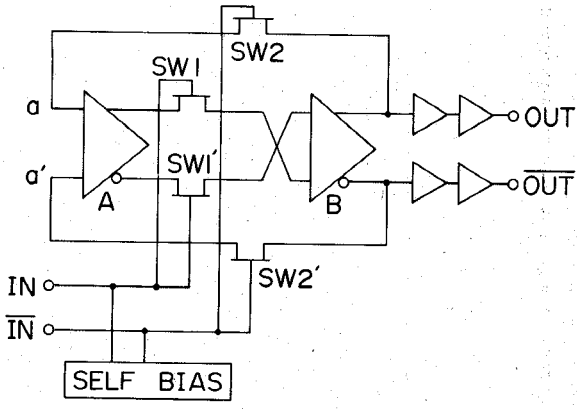

Fig. 1. Circuit configuration of dynamic frequency divider.

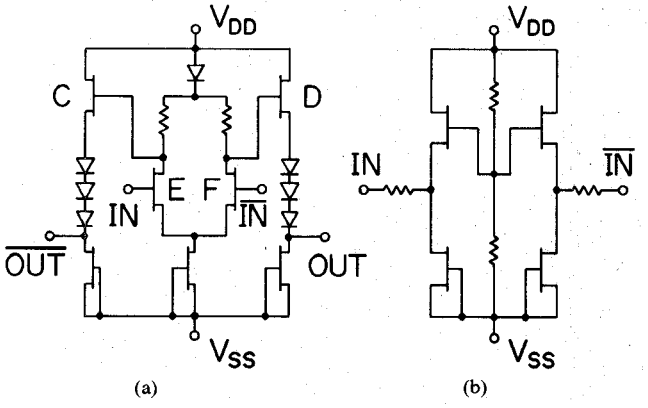

Fig. 2. (a) Circuit configuration of differential amplifier. (b) Circuit configuration of self-bias circuit.

providing the high output impedance to the divider. Moreover, a double-loop structure was adopted for stabilizing the operation.

There are many advantages to this design.

1) The differential amplifier and self-bias circuit permit operation with a single voltage power supply.
2) The double-loop structure provides fast operation of the differential amplifier. Also this structure provided the same delay to the invert and the same phase output.
3) Because the differential amplifier evaluates the relative voltage of points a and a' (Fig. 1), fluctuation of their absolute voltages does not hinder successful operation.
4) The self-bias circuit provided a suitable operating dc level when the supply voltage was changed.
5) The gain of the buffer circuit (differential amplifier B in Fig. 1) increases the loop gain, permitting low voltage supply operation.
6) The multistage frequency divider was easy to construct, because 0° and 180° phase outputs were obtained by using this divider. These two phase outputs were used as clock and inverted clock for the next stage divider. Conventional dynamic dividers require additional circuit to produce 0° and 180° output.

To design the circuit parameters, we first calculated the optimum dc input bias by decomposing the divider. Namely, the loop was cut at points a and a', and one side of the cut was connected to input signals and the other side was connected to the differential amplifiers for the load of switch SW2. Two different supply voltages were selected, -5 V and -7 V.

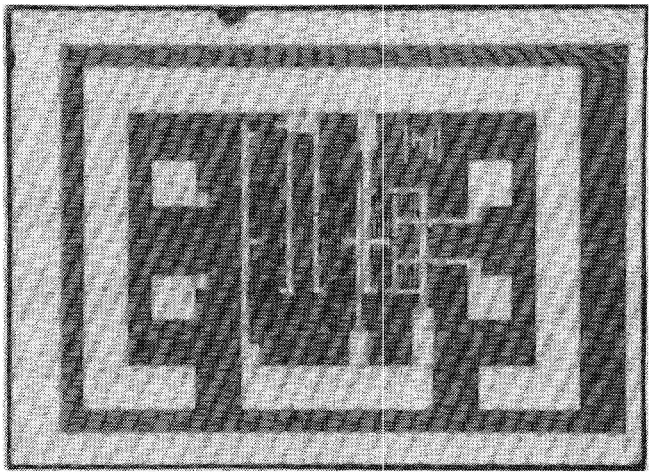

Fig. 3. Micrograph of the dynamic frequency divider.

The other circuit conditions were as follows: the gate length was 1.0 μm, the gate width was 40 μm, and the load resistance of the differential amplifier was 0.9 kΩ. The gate width of the last stage output buffer was 80 μm. The threshold voltages of the FET's were used -0.8 V and -0.4 V. To obtain high sensitivity, low-threshold-voltage FET's (-0.4 V) were used as the switch FET's and input FET's of the differential amplifier (E and F in Fig. 2), because low threshold voltage FET's have greater transconductance. Then the characteristics of the divider were calculated using the simulation program SPICE.

For a -5 V supply voltage, with the input bias level properly set, and a 1 V_{p-p} input signal, the on-to-off ratio of the circuit gain was 20 dB at 6 GHz, and 8 dB at 2 GHz. The maximum loop gain was 20 dB. The loop gain cutoff frequency (0 dB) was 7.6 GHz and 9 GHz when the input level was -4.0 V and -3.5 V, respectively. This frequency varied with the input signal power. The simulation revealed that this type would be able to operate from 2 GHz to 9 GHz, when the input dc level was adjusted to -3.5 V.

At -7 V the frequency divider was designed to operate at a higher operating frequency. The divider was able to operate from 6 GHz to 11 GHz, when the input self-offset voltage was adjusted to -3.6 V.

III. Experimental Results

The LDD (lightly-doped-drain) structure WSi self-alignment process gate technology was used for IC fabrication with a gate length of 1.0 μm. The threshold voltages were -0.8 V and -0.4 V. Fig. 3 is a micrograph of the frequency divider. The chip size is 1.2 mm $\times$ 1.4 mm.

Fig. 4 shows the input sensitivity characteristics of the frequency divider. Stable operation was observed from 2.0 to 8.0 GHz when the input power was 5 dBm. The supply voltage was -5 V, and the divider operated stably under even ± 10 percent supply voltage fluctuations. Power dissipation was 370 mW. With the -7 V supply voltage, at the same input power (5 dBm), operating frequencies were 6.0 to 10.5 GHz, as shown in Fig. 5. This operation was also stable for ± 10 percent supply voltage fluctuations. Fig. 6 shows the input and output waveforms at 9 GHz. Conventional dynamic frequency dividers change their operating frequency region when the supply voltage fluctuates.

A static frequency divider, fabricated on the same wafer, operated up to 6.5 GHz. Thus this shows that the dynamic divider using differential amplifiers was faster than the static one.

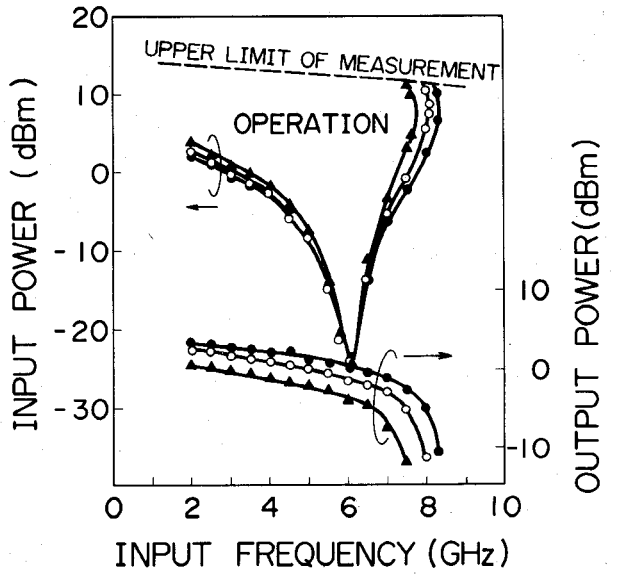

Fig. 4. Frequency characteristics at different supply voltages. Triangles mark data recorded for operation at −4.5 V, open circle at −5.0 V, and closed circle at −5.5 V.

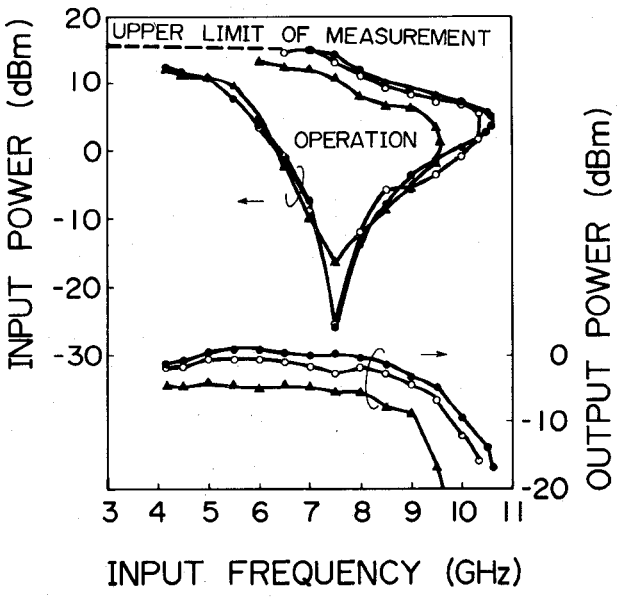

Fig. 5. Frequency characteristics at different supply voltages. Triangles mark data recorded for operation at −6.3 V, open circle at −7.0 V, and closed circle at −7.7 V.

IV. Summary

New 2.0–8.0 GHz and 6.0–10.5 GHz dynamic frequency dividers have been developed. The divider was constructed with a double-loop connected pair of differential amplifiers. The frequency divider was operated from one voltage supply at −5 V, or −7 V with ±10 percent voltage supply fluctuation. This divider overcomes the weak points of conventional dynamic dividers, which need two voltage supplies and precise supply voltage control. This divider operates at a 50 percent higher frequency than static dividers.

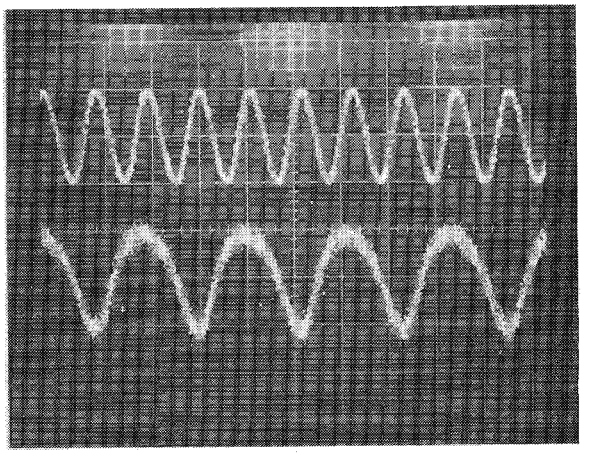

Fig. 6. Input and output waveforms of the frequency divider. Top: input waveform. Bottom: output waveform. 20 dB attenuator inserted between D.U.T. and sampling oscillator. Vertical axis: 50 mV/div. (input); 10 mV/div. (output). Horizontal axis: 100 ps/div.

Acknowledgment

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Properties of Shielded Cylindrical Quasi-TE_{0nm}-Mode Dielectric Resonators

JERZY KRUPKA

***Abstract*—Comparison of the Rayleigh–Ritz method and the mode-matching method for computations of quasi-TE_{0nm}-mode frequencies and unloaded Q factors of shielded dielectric resonators is presented. Rigorous bounds for the true quasi-TE_{0nm}-mode frequencies are assessed. Influence of various parameters on the resonant frequencies, unloaded Q factors, and the temperature coefficients of the resonant frequency is demonstrated for many shielded dielectric resonator structures. Different approaches to unloaded Q factor computations are discussed and numerically compared.**

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